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Using Transformer in Low Noise Phase Quadrature VCO

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ABSTRACT

This paper aims to introduce a quadrature VCO which applies superharmonic coupling. The presented quadrature VCO is suitable to be used, both with 2×subharmonic mixers, as well as 4×subharmonic mixers. It would be impossible to avoid the presence of harmonics in GaAs HEMT VCO circuits. These harmonics are in general, undesirable signals which tend to accompany the desired fundamental signal. There are common-mode nodes (similar to those in the two source nodes in a cross-coupled VCO) in deferential VCO at which higher-order harmonics are present while the fundamental is absent in essence. We can make use of these second-order harmonics which are present at the common-mode nodes of two VCO in order to to implement a quadrature connection between the fundamental outputs. The technique through which this is done is called superharmonic coupling. This GaAs HEMT quadrature VCO which applies active superharmonic coupling puts an excellent performance in show, with an output power -0.942dBm for fundamental and -9.751dBm for subharmonic, phase noise -107.2dBc/Hz for fundamental and -114.8dBc/Hz at a 1MHz offset. All of circuit applied are designed and simulated by ADS, 2008.

Keywords: *Quadrature VCO ,Cross-Couple,Phase Noise, GaAs HEMT*

1. INTRODUCTION

The rapid growth of new generation of wireless communication systems has created a high demand for designing single-chip radio transmitter and receiver devices in a fully integrated CMOS process with a very small size due to better combination, lower cost and lower operating voltage. To increase the combination and integration level, all passive components should be combined integrated in a single chip. In this case, elements of a LC intensified circuit in an voltage controlled oscillator (VCO) as a core part of combinatory must have high Q coefficients in frequency setting range. In this chapter, technological aspects of mouse verector implementation and spiral inductions, main concepts of circuit design and circuit implementation issues, oscillator phase noise and the effect of low frequency filker noise are discussed. Several practical examples of CMOS Quadrature voltage controlled oscillators are also presented using different process technologies.

Oscillators are fundamental components in wireless communications systems that can be used for several applications. Communication systems that use phase shift keying modulation frequently require a pair of LO signals that are in quadrature, or 90° out- of-phase.

Quadrature VCO is one of the most important components in direct conversion transceivers. These VCOs are of a basic role in image-rejection techniques which are based on the appropriate phasing of the signals. Furthermore, they eliminate the immense and non-planar high-frequency filters. It also should be added that, some digital radio communication systems (e.g. GSM and DECT) in which complex digital modulation schemes are applied in order to reduce the signal bandwidth to the possible minimum level, need quadrature VCO [1]. In all the applications mentioned above, departures from the quadrature phase or the existence of an amplitude imbalance between the two signals leads to a damaging effect on the performance of the whole system. There are a number of techniques which can be applied to produce quadrature signals.

1) The first technique is a standard VCO which a RC-CR phase-shift network follows. If the real values of R and C are not accurate, it may result in errors in the quadrature which, in turn, necessitate compensation of some form [2].

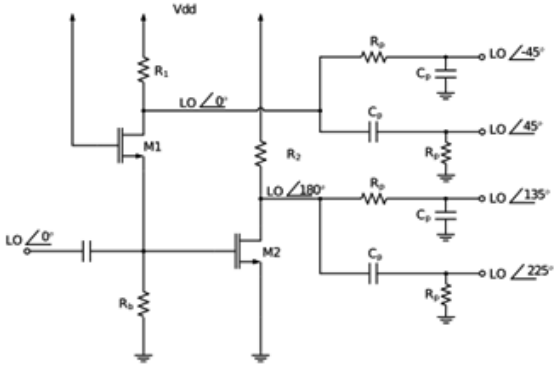

Figure 1: RC-CR Phase-Shift Network

2) The second technique which can be applied is a VCO which runs at double frequency and a digital frequency divider based on flip-flops follows it. Here, the sections of the circuit which work at the double frequency may turn into a speed or power bottleneck.

3) Another technique is employing two cross-coupled VCO's [3].

4) Using active polyphase filters such as ring oscillator designs is another technique in this list. In four-delay stage ring oscillators, for example, taps at diametrically opposite points yield quadrature phases [4].

An alternative method for obtaining quadrature VCO based on the differential coupling at the second harmonics of two differential VCOs is introduced in this paper. As a matter of fact, if s 180-degrees phase shift occurs between the second harmonics of two VCOs, their basic frequency components will be in quadrature states.

2. CHALLENGES AND PROBLEMS OF CMOS

As mentioned in the section of introducing different structures of the oscillator, one of the fundamental problems of CMOS technology at high frequencies is low mutual conductivity and signal loss through conductive silicone substrate. Basically, achieving low noise and high gain for the oscillator deal with power loss, which is not desirable for portable wireless systems. Most high gain amplifier topologies are proposed to eliminate the need for low power loss for one of more efficient features such as cascade amplifier and inverted amplifier.

Also the market demand for advanced communication systems implies the performance at low bias conditions for low noise amplifier. Applying one volt input voltage and less is very important in explaining RF digital and analog circuits. When there is a gain more than 10 db, noise number should not exceed 3 db. Most topologies for oscillators are of cascade type; this topology has a high gain, low noise and sufficient separation between input and output but is not suitable for low voltage source.

Using a single MOS is appropriate for low voltage application, but it does not establish between input and output because by increasing work frequency of over-lap capacitor, field-effect gate-drain transistor (Cgd) plays an important role in the; because its value is comparable with gate-source capacitor in deep-submircron CMOS technology.

GaAs technology is used for designing. This transistor has better advantages and fewer problems than CMOS technology transistors which can refer to higher gain and higher possibility of linearization. In this chapter, first, initial definitions about major factors of designing an amplifier are discussed and in the following step by step designing and their simulations.

3. DESIGN OF A 4.8 GHZ VCO

The cross-coupled VCO is the most frequently used microwave VCO topology in GaAs technology. We can prepare a model of a LC VCO with the capacitor and inductor, parallel with a resistor to simulate the losses in the tank, and also a negative resistance to simulate the active device. in order to produce the negative resistance to compensate for the losses in the LC tank, employing a cross-coupled differential pair, as shown in Figure2, would be a choice. The resistance, R_{in} looking into the cross-coupled pair is obtained by:

$$R_{in} = -\frac{2}{g_m} \qquad (1)$$

g_m is the transconductance of each of the FETs in the cross-coupled pair.

Therefore, by choosing a proper device size and biasing, the value of negative resistance necessary to counteract, we are able to find the losses in the tank.

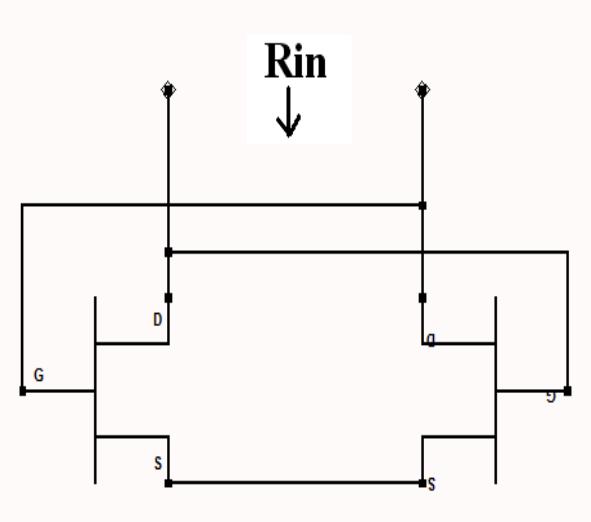

Figure 2: Negative Resistance generated from Cross-Coupled FET

Figure 3 illustrates a frequently employed LC VCO circuit using the cross coupled differential pair. A moderately low supply voltage is possible to be used for this implementation because there are only two levels of transistors. However, it calls for two inductors, which require considerable chip area.
The VCO topology illustrated in Figure3 was applied (with FET transistor) in [5].

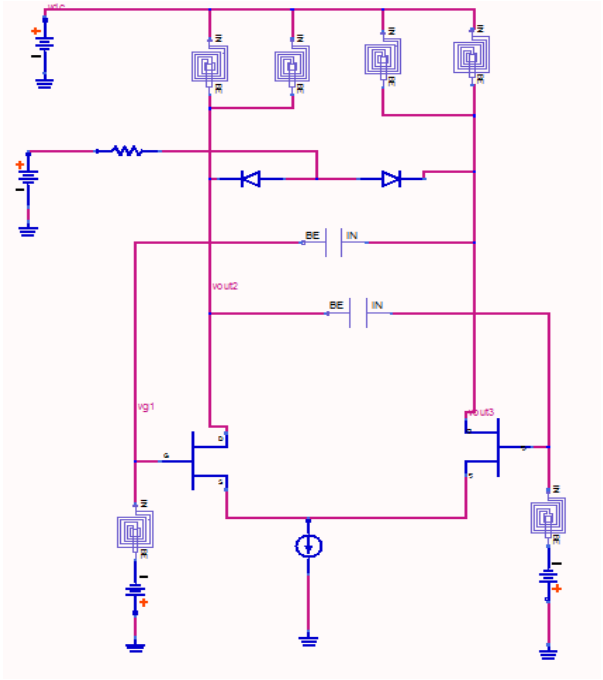

Figure 3: Cross-coupled FET VCO

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GaAs HEMT technology was applied to design fundamental C band VCO for the present experiment. The Diode varactor illustrated in Figure2 allows the tuning of frequency. The signal output power was about942dBm and the phase noise at a 1 MHz offset was -107.2dBc/Hz.

Figure 4 illustrates the phase noise graph. Figure 5 illustrates the output power spectrum and figure 6 illustrates Time-domain VCO outputs.

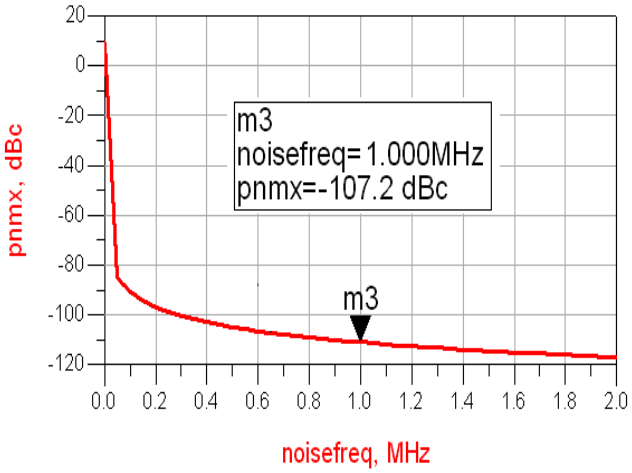

Figure 4: Phase Noise 4.8GHz VCO

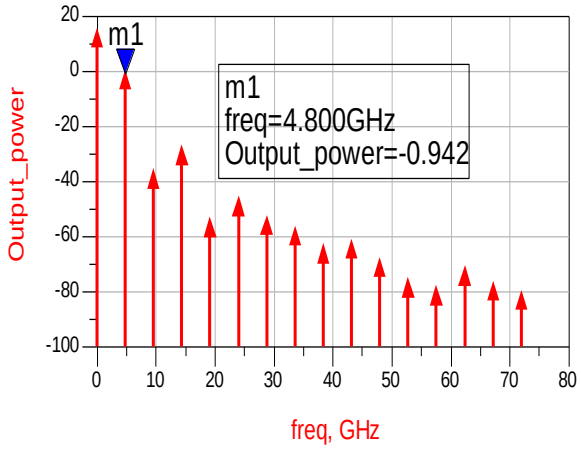

Figure 5: Output Power VCO

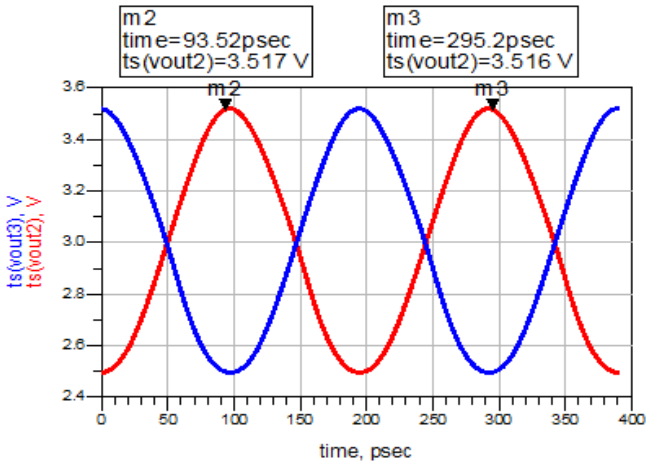

Figure 6: Time-domain VCO Outputs

4. CONCEPT OF THE QUADRATURE VCO

In most GaAs processes, resistors are particularly of large tolerances. Hence, this method may result in a low degree of accuracy in the quadrature signals that generated. In order to generate quadrature signals, another method is to employ a digital frequency divider which follows a VCO running at the frequency two times larger than the fundamental frequency [6]. There are some essential restrictions against using this technique at high frequencies for it calls for a VCO operating at double the desired frequency. A third frequent technique is to force two VCOs to run in quadrature through applying coupling transistors running at the fundamental frequency [7]. The problem with this technique is a trade-off between quadrature accuracy and phase noise which is due to the effects the coupling circuit imposes on the oscillation frequency. In order to overcome this problem, we may take advantage of realizing a quadrature VCO through superharmonic coupling. As shown in Fig.7a, quadrature signals are produced at the fundamental frequency by using differential coupling at the common-mode nodes where the

second harmonic is predominant. In order to implement the coupling of the second harmonic with a 180° phase shift, the on-chip transformer has been inverted [8]-[10] (Fig.7b).

The method of superharmonic coupling implements a 180^0 connection between the even-ordered harmonics of the two VCO circuits, and this happens while both passive and active superharmonic coupling circuits are achievable. The performance of the two individual deferential VCOs, as alongside with the coupling network will determine the performance of a quadrature VCO which applies the superharmonic coupling topology. This results in an anti-phase relationship between the second-order harmonics at the common-mode nodes.

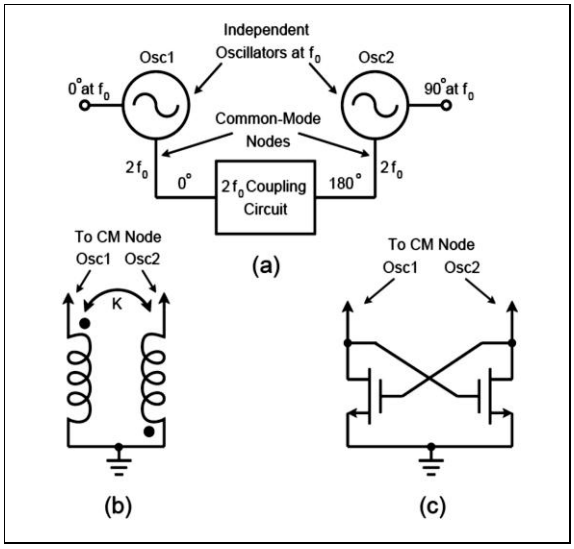

Figure 7. (a) Superharmonic coupling of the second harmonic to enforce quadrature at the fundamental. (b) Coupling using an inverting transformer. (c) Coupling using a cross-coupled pair

In [8], active super harmonic connection with chip transducer at 0.35 μm technology has been used to establish Quadrature relation between the two oscillators. This VCO could be set from 4.57 GHz to 5.21 GHz and reached -138 dBC phase noise at 1 MHz error. Output signal power was -9 dBm, DC power consumption of oscillator center 5.1 mw and chip dimensions 1250 μm ×1250 μm. The disadvantages of active super harmonic connection technique in general are that chip transducers consume a dramatic area of the chip and have a limited Q factor especially at CMOS technology.

A method of replacing the transducer with cross-coupled differential was presented in [9], which greatly reduces the required chip area. In [9] the Quadrature voltage controlled oscillator at 6 GHz in SiGe technology was proposed with the connected circuit of figure c4-6 with two oscillators in figure 4-4. The estimated output power was -5.3 dBm and setting range was 24% phase noise was estimated up to -105.8 dBc at 1 MHz error.

5. PROPOSED QUADRATURE VCO

A frequently method used for implementing a GaAs HEMT differential LC VCO is applying a cross-coupled pair for generating the negative resistance needed for compensating for the losses in the tank. Hence, by choosing the proper device size and biasing, we are able to realize the negative resistance needed to counteract the losses in the tank. The core quadrature VCO circuit investigated in this work is shown in **Figure 8** . It is made of two cross-coupled VCOs which are linked via an inverting transformer. It has been shown that the phase noise of the VCO can be enhanced notably by including cross-coupled inductor above the cross-coupled NMOS transistors, due to the higher transconductance and faster switching speed of the corresponding structure [10]. We can find the oscillation frequency for each VCO via the common formula for finding the resonant frequency of an LC tank, in which L is the value of the on-chip spiral inductor and C is the total capacitance at the tank nodes. The inductors employed in this circuit of the capacitance less than 1.5nH. The overall capacitance, including the lumped capacitor, and adding the parasitic capacitance was 0.855pF which provided oscillation at 4.8GHz.

The network which is employed to implement the 180^0 phase difference in the second-order harmonics is a vital component of the quadrature VCO. This anti-phase association is the factor which generates the quadrature phase relationship at the fundamental frequency. Convenient common-mode nodes which are used for coupling the second harmonic are the common source nodes in each of the cross-coupled differential pairs, which are signified by CM1 and CM2 in the comprehensive VCO circuit schematic illustrated in Figure8. Owing to the fact that any practical use of a VCO requires connecting its output to other circuitry, buffers are required to be employed in order to guarantee that loading does not disrupt the oscillations. For each of the four outputs we have used source follower buffers that we were able to measure the VCO using equipment with $50\,\Omega$ input impedances. The 180^0 and 270^0 outputs were terminated on-chip with $50\,\Omega$ loads and the 0^0 and 90^0 were linked to CPW pads for on-chip inquiring.

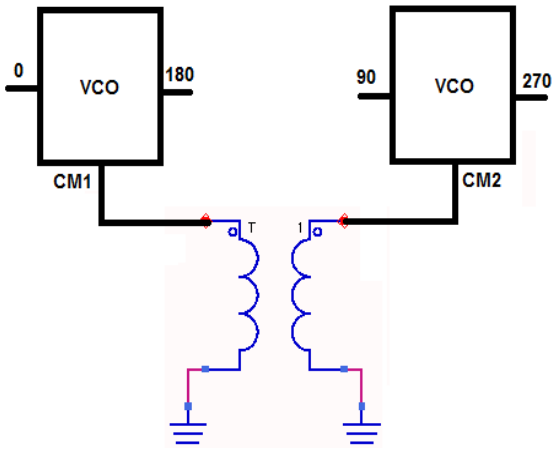

Figure 8: Schematic Quadrature VCO

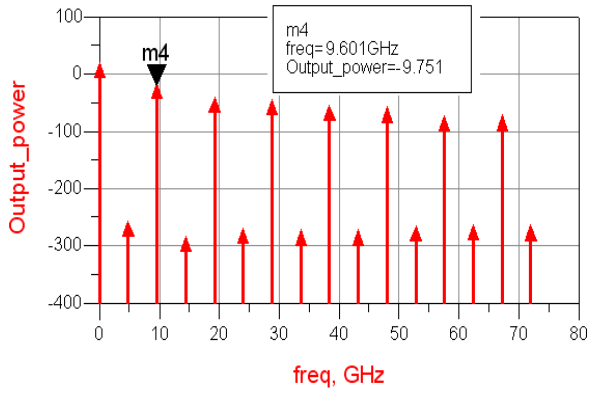

Figure 9: Output Power Quadrature VCO

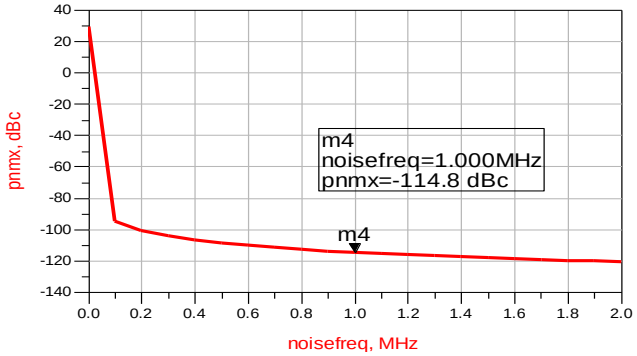

Figure 10: Phase Noise Quadrature VCO

In Quadrature VCO at subharmonic frequency (9.6GHz) the signal output power was approximately -9.751dBm and the phase noise at a 1 MHz offset was -114.8dBc/Hz.

Figure9 shows spectrum of output power Figure10 shows Graph of phase noise. And figure11 shows Time-domain VCO outputs. Table 1 shows result of fundamental and subharmonic VCO.

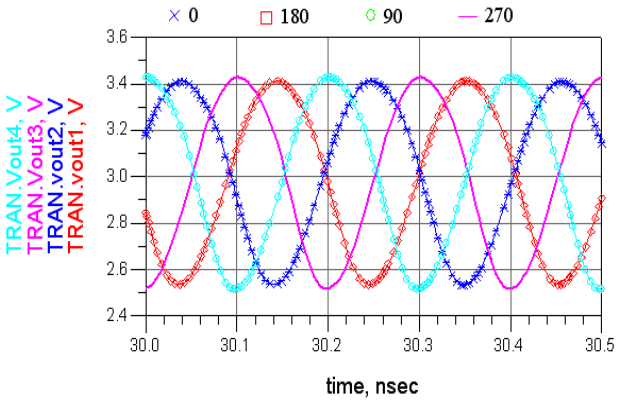

Figure 11: Time-domain Quadrature VCO

TABLE I. COMPARE FUNDAMENTAL AND SUBHARMONIC VCO.

	Fundamental	**Subharmonic**
Freq	4.8GHz	9.6GHz
Output Power	-0.942dBm	-9.751dBm
Phase Noise	-107.2 dBc/Hz	-114.8 dBc/Hz

6. CONCLUSION

This paper represents a GaAs HEMT quadrature VCO which was designed at 4.8 GHz by applying superharmonic coupling. This technique focuses on coupling the second-order harmonics between two VCO and obliges an anti-phase connection, which, in turn, compels a quadrature relationship at the fundamental. In order for this coupling with a 180^0 phase shift to be implemented, a cross-coupled differential NPN pair was employed at the common-mode nodes. This GaAs HEMT quadrature VCO which employs an active superharmonic coupling demonstrates a very fine performance with an output power of -0.942dBm for fundamental and -9.751dBm for subharmonic, phase noise of -107.2dBc/Hz for fundamental and -114.8dBc/Hz at a 1MHz offset. it creates the 180^0 phase shift in the second-order harmonics by using an inverting transformer.

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