



Quantum Cost Optimization for Reversible Carry Skip BCD Adder

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ABSTRACT

Reversible Logic is a very promising and flourishing research area. Reversible logic theoretically allows designers to build subsystem circuit design with zero power dissipation than the existing classical ones. However synthesis of reversible circuit is not easy. In this paper we propose an efficient approach for carry skip BCD adder using reversible logic. Our results show that our design is much more efficient than the existing ones in terms quantum cost, garbage outputs and delay.

Keywords: Adder, BCD Adder, Garbage Output, Reversible Logic, Quantum Cost.

1. INTRODUCTION

In recent year reversible logic has received great attention of the researchers. The primary reason for this is the increasing demands for lower power devices. In early 1960s R. Landauer [1] demonstrated that losing bits of information causes loss of energy. Information is lost when an input cannot be recovered from its output. In 1973 C. H. Bennett [2] showed that energy dissipation problem can be avoided if the circuits are built using only reversible logic gates. Reversible logic gates have a one to one mapping between its inputs and its outputs. So no information bit lost and therefore no loss of energy [3].

In current literature most of the researchers realized complex gate using realizable gates and the cost is significantly high. They used the circuit as a single gate in their design to claim success in terms of number of gates. Although the number of gates is proposed as a major metric of optimization [4], Dmitri Maslov et al.[5] proved that number of gates is not a good metric of optimization as reversible gates are of different type and have different quantum costs. In this paper we propose a novel design of carry skip BCD adder that is efficient in terms of quantum cost, number of garbage outputs and delay.

The rest of the paper is organized as follows. In Section 2 we present some basic definitions related to reversible logic. Section 3 covers description of basic reversible logic gates and their quantum implementation. Section 4 describes the logic synthesis of proposed carry skip adder circuits and compares our design with other researchers. Finally this paper is concluded with Section 5.

2. BASIC DEFINITIONS

In this section, some basic definitions related to reversible logic are presented. We formally define reversible gate,

garbage output, delay in reversible circuit and quantum cost of reversible in reversible circuit.

2.1 Reversible Gate

A Reversible Gate is a k-input, k-output (denoted by k*k) circuit that produces a unique output pattern for each possible input pattern [6]. If the input vector is I_v where $I_v = (I_{1,j}, I_{2,j}, I_{3,j}, \dots, I_{k-1,j}, I_{k,j})$ and the output vector is O_v where $O_v = (O_{1,j}, O_{2,j}, O_{3,j}, \dots, O_{k-1,j}, O_{k,j})$, then according to the definition, for each particular vector j , $I_v \ll O_v$.

2.2 Garbage Output

Every gate output that is not used as input to other gates or as a primary output is garbage. Unwanted or unused outputs which are needed to maintain reversibility of a reversible gate (or circuit) are known as Garbage Outputs. The garbage output of Feynman gate [7] is shown Figure 1 with *.

2.3 Delay

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. The definition is based on two assumptions: (i) Each gate performs computation in one unit time and (ii) All inputs to the circuit are available before the computation begins. In this paper, we used the logical depth as measure of the delay proposed by Mohammadi and Eshghi [8]. The delay of each 1x1 gate and 2x2 reversible gate is taken as unit delay 1. Any 3x3 reversible gate can be designed from 1x1 reversible gates and 2x2 reversible gates, such as CNOT gate, Controlled-V and Controlled-V⁺ gates (V is a square-root-of NOT gate and V⁺ is its hermitian). Thus, the delay of a 3x3 reversible gate can be computed by calculating its logical depth when it is designed from smaller 1x1 and 2x2 reversible gates.

Quantum Cost

The quantum cost of a reversible gate is the number of 1x1 and 2x2 reversible gates or quantum gates required in its design. The quantum costs of all reversible 1x1 and 2x2 gates are taken as unity [9]. Since every reversible gate is a combination of 1 x 1 or 2 x 2 quantum gate, therefore the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V⁺ and CNOT gates used.

3. QUANTUM ANALYSIS OF POPULAR REVERSIBLE GATES

Every reversible gate can be calculated in terms of quantum cost and hence the reversible circuits can be measured in terms of quantum cost. Reducing the quantum cost from reversible circuit is always a challenging one and works are still going on in this area. This section describes some popular reversible gates and quantum equivalent diagram of each reversible.

3.1 Feynman Gate

Let I_v and O_v are input and output vector of a 2*2 Feynman gate where I_v and O_v are defined as follows: $I_v = (A, B)$ and $O_v = (P = A, Q = A \oplus B)$. The quantum cost of Feynman gate is 1. The block diagram and equivalent quantum representation for a 2*2 Feynman gate are shown in Fig. 1.

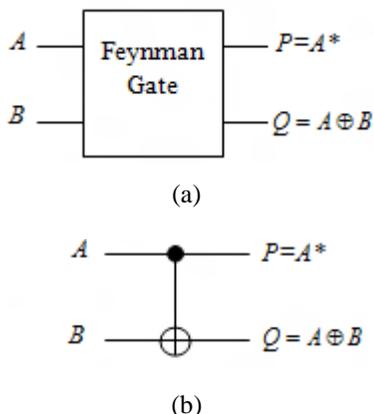


Fig. 1. (a) Block diagram of 2x2 Feynman gate and (b) Equivalent quantum representation.

3.2 Double Feynman Gate

Let I_v and O_v are input and output vector of a 3*3 Double Feynman gate (DFG) where I_v and O_v are defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A, Q = A \oplus B, R = A \oplus C)$. The quantum cost of Double Feynman gate is 2 [10]. The block diagram and equivalent quantum

representation for 3*3 Double Feynman gate are shown in Fig. 2.

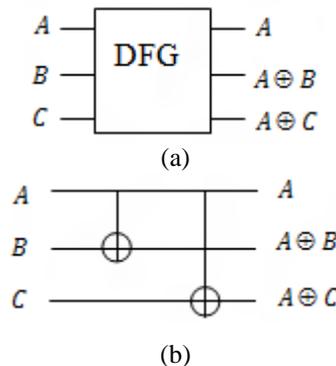


Fig. 2. (a) Block diagram of 3x3 Double Feynman gate and (b) Equivalent quantum representation.

3.3 Toffoli Gate

The input vector, I_v and output vector, O_v for 3*3 Toffoli gate (TG) [11] can be defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A, Q = B, R = AB \oplus C)$. The quantum cost of Toffoli gate is 5. The block diagram and equivalent quantum representation for 3*3 Toffoli gate are shown in Fig. 3.

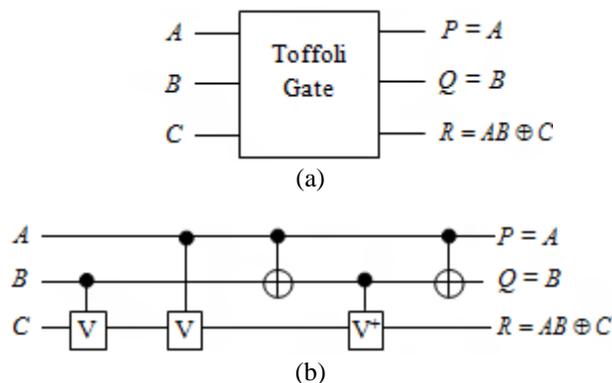
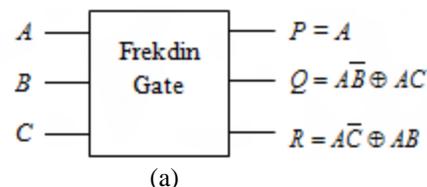


Fig.3. (a) Block diagram of 3*3 Toffoli gate and (b) Equivalent quantum representation.

3.4 Frekdin Gate

The input vector, I_v and output vector, O_v for 3*3 Fredkin gate (FRG) [12] can be defined as follows: $I_v = (A, B, C)$ and $O_v = (P=A, Q = \bar{A}B \oplus AC, R = \bar{A}C \oplus AB)$. The quantum cost of Frekdin gate is 5. The block diagram and equivalent quantum representation for 3*3 Fredkin gate are shown in Fig. 4.



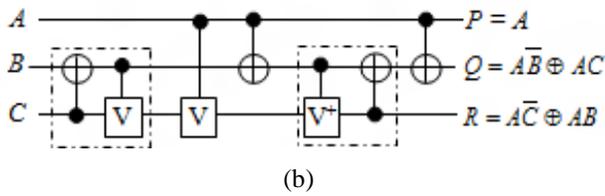


Fig.4. (a) Block diagram of 3*3 Frekkin gate and (b) Equivalent quantum representation

3.5 Peres Gate

The input vector, I_v and output vector, O_v for 3*3 Peres gate (PG)[13] can be defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$. The quantum cost of Peres gate is 4. The block diagram and equivalent quantum representation for 3*3 Peres gate are shown in Fig. 5.

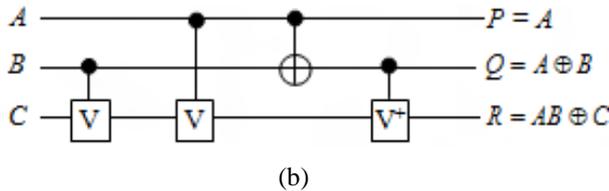
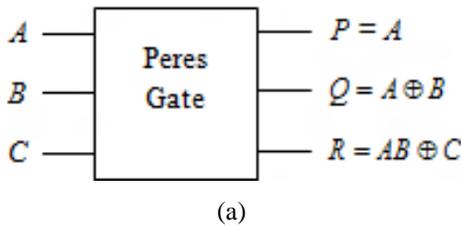


Fig.5. (a) Block diagram of 3*3 Peres and (b) Equivalent quantum representation

4. PROPOSED CARRY SKIP ADDER

In this section we first present our proposed design for all the components of carry skip adder and then describe our proposed novel design of carry skip adder that is optimized in terms of quantum cost, delay and garbage outputs.

4.1 Proposed Full Adder Block

Our proposed full adder block is shown in figure 6(a). It is realized by two Toffoli gates and two Feynman gates and its quantum cost is $2*5$ (quantum cost of TG is 5) $+2*1$ (quantum cost of FG is 1) $=12$. Quantum implementations of our adder block and cost minimization using template matching and moving rules are shown in figure 6(b) to figure 6(d). Finally the cost is reduced to 6.

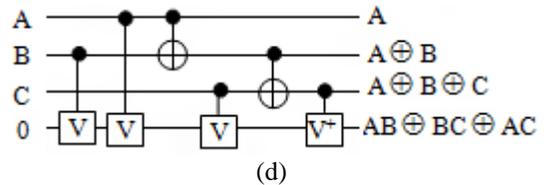
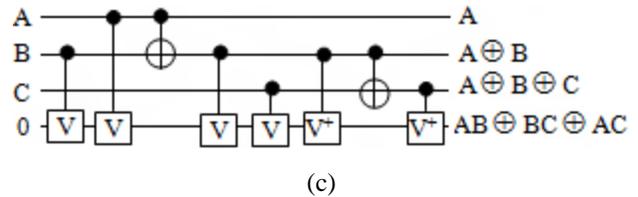
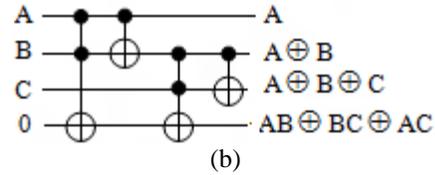
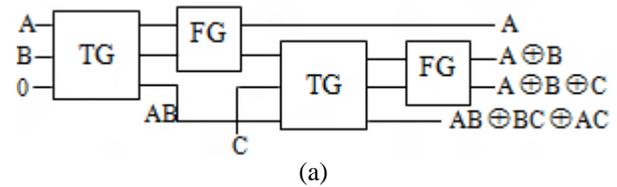


Fig.6. Block diagram of the proposed full adder block and its equivalent quantum implementation.

4.2 Proposed Multiplexer Block

For multiplexer block we modify the Frekkin gate. The input vector, I_v and output vector, O_v for 3*3 modified Frekkin Gate (MFRG 1) is defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A, Q = A \oplus \overline{AB} \oplus AC = \overline{AB} \oplus \overline{AC}, R = \overline{AC} \oplus AB)$. The quantum realization of MFRG1 is shown in figure 7(a) and 7(b). Here input A works as a selector and B and C as mux inputs to be selected by A. When A=0 the 3rd output is C and when A=1 the 3rd output is B. The quantum cost of Modified FRG1 gate is 4, delay 4 and it produces 2 garbage outputs.

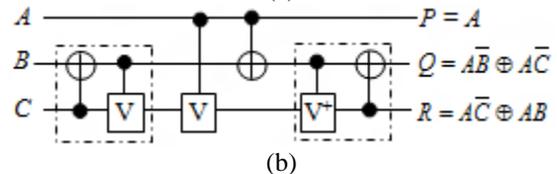
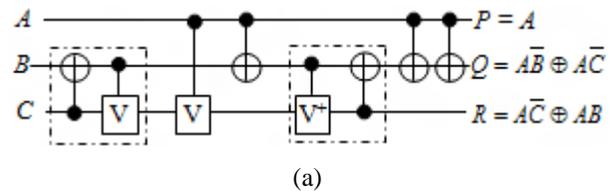


Fig.7. Equivalent quantum representation of MFRG1 gate.

4.3 Proposed Carry Propagation Block

On the design of carry propagation block we consider the block size 4. Carry propagation block receives 4 inputs P_0, P_1, P_2 and P_3 and we have to generate $P_0P_1P_2P_3$. It can be realized by three Peres gates. Our proposed carry propagation block is shown in figure 8 producing 6 garbage bits and 12 (= 3*4, quantum cost of PG is 4) quantum cost.

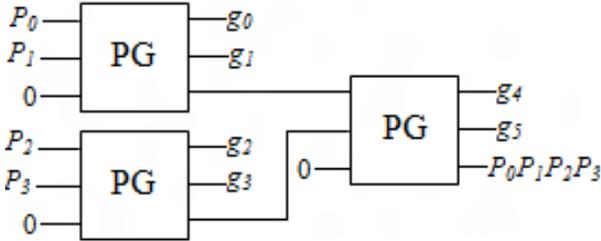
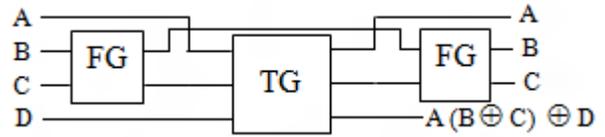


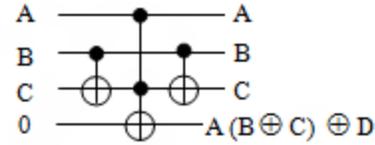
Fig. 8. Proposed carry propagation block

4.4 Proposed Correction Logic Block

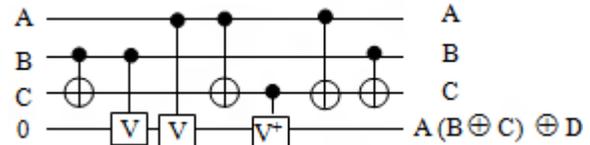
The correction logic block receives carry C_4 and three sums S_1, S_2 and S_3 as inputs. The required logic for the correction block is $C_4 \oplus S_3 (S_1 \oplus S_2)$. Our proposed reversible logic circuit for correction block is shown in figure 9(a). It can be realized by giving S_3, S_2, S_1 and C_4 as inputs to the 1st (=A), 2nd (=B), 3rd (=C) and 4th (=D) inputs to the block. The 4th output will generate $C_4 \oplus S_3 (S_1 \oplus S_2)$. The quantum equivalent circuits for the correction block are shown in figure 9(b) to 9(c). The quantum cost of the proposed logic block is 7.



(a)



(b)



(c)

Fig.9. Proposed correction logic design and its equivalent quantum representation

4.5 Proposed Carry Skip Adder

Our proposed carry skip adder is shown in figure 10. It is realized by 5 full adder blocks, one carry propagation block, one correction logic block, one 2 to 1 multiplexer block, one Peres gate and 2 Feynman gates. The overall quantum cost of our proposed BCD carry skip adder is 5*6 (5 full adder blocks) + 4*1(1 multiplexer block) + 12*1(1 carry propagation blocks) 7*1 (1 correction logic block) + 4*1(1 Peres gate) + 1*2(2 Feynman gates) = 59. The total number of garbage outputs is 6(shown in figure 8) + 6(from carry propagation blocks) + 2(from MUX) =14.

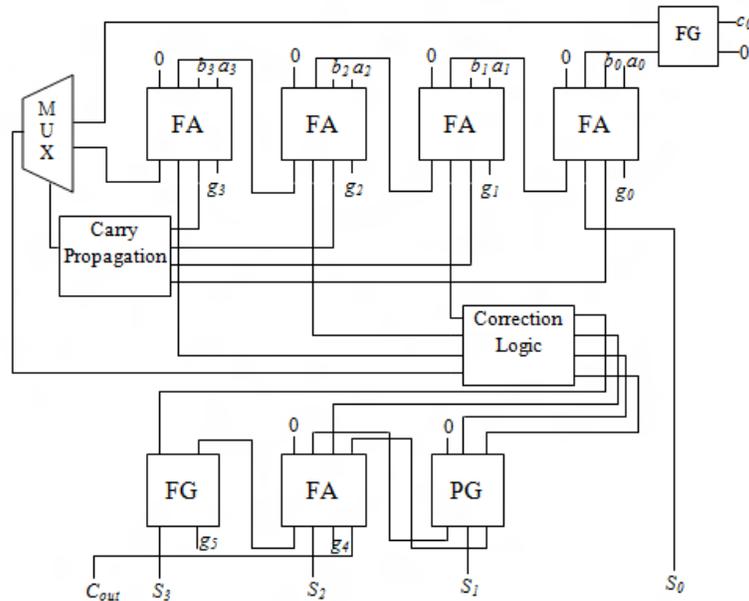


Fig.10. Proposed design of BCD carry skip adder.

In [14] 3 New gates (NG) for the correction logic circuit and 8 TSG gates for the adders are used for the

construction of reversible implementation of BCD adder. The quantum cost of the design is 129. This produces 27

garbage outputs with 11 constant inputs. But in this paper fan-out is not taken into account which when considered will increase the number of gates and quantum cost.

In design [15] a 4 bit parallel adder constructed using four TSGs and a FG to fan out C_{in} . The design uses two Fredkin gates and one Toffoli gate for the correction logic. It uses a combination of one FG, one PG and a TSG for the adder-2 block which adds the C_{out} to the sum in order to generate the final BCD sum. To generate block generation bit P three FRGs are used. Finally to generate C_{out} and to fan-out three sum bits, another three FRGs and a TG are used. This implementation requires a total of 101 quantum cost and it produces a total number of 15 garbage outputs with 11 constant inputs.

The implementation of design [16] uses 5 TSGs for both adders, 3 NGs for correction logic, one MTG for multiplexer block and one Feynman gate for fanout. It uses one 6 inputs Toffoli gate for carry propagation logic which optimizes the number of gate counts but increase the quantum cost. The total quantum cost of the design is 137 and it produces 14 garbage outputs.

In [17] 8 TSGs used for adders, 3 NGs are for correction logic and 2 FRGs and 1 TSG for carry propagation logic. The quantum cost of the design is 151 and produces 27 garbage outputs. The comparisons of our design with the existing ones in literature are summarized in table 1.

Table 1. Comparisons of Different Designs of Carry Skip BCD Adders

Carry Skip BCD Adder	Cost Comparisons		
	Quantum Cost	Garbage Outputs	Delay
Proposed	59	14	59
Existing [14]	129	27	129
Existing [15]	101	14	101
Existing [16]	137	14	137
Existing [17]	151	27	151

5. CONCLUSION

Reversible carry skip BCD adder is a very important subsystem for the forthcoming quantum devices. In this paper we proposed an optimized design for reversible carry skip BCD adder. Appropriate algorithms and theorems are presented to clarify the proposed design and to establish its efficiency. We compare our design with existing ones in literature which claims our success in terms of number of gates, number of garbage outputs and delay. This optimization can contribute significantly in reversible logic community.

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